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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,665	08/31/2001	Toshiharu Furukawa	BUR919990305US1	3799

7590            07/30/2003  
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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/944,665	FURUKAWA ET AL.
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears in the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 29 April 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) 11-17 is/are withdrawn from consideration.
- 5) Claim(s) 18-28, 31-39 and 41-44 is/are allowed.
- 6) Claim(s) 1-10, 29, 30, 40 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

1. Claims 3, 8 and 10 are objected to because of the following informalities: Claim 3, line 4, the phrase "said insulator" is unclear whether it is being referred to the layer of insulator or the insulator material of claim 1. Claim 8, line 4, the phrase "said insulator" is unclear whether it is being referred to "said insulator material". Since there is no claim 61 in the application, it is unclear whether claim 10 depends to claim 6.

Appropriate correction is required.

2. Claims 29, 30 and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 29, line 2, the phrase "said gate structure is borderless to said second diffusion" is unclear as to how the gate structure is borderless to the second diffusion. Figs. 23C and 37C shows the gate structure is border to the second diffusion. It is believed that the gate contact is borderless to the second diffusion.

Since a spacer is different from the contact, it is unclear how the contact to said second diffusion comprises a spacer self-aligned to said edge in claim 30.

Claim 40, line 2, the phrase "sub-lithographic width" is unclear as to what is the actual width of the channel as compare to the other structures of the device.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 23, lines 2-3, the phrase "said gate structure extends on at least three sides of said channel". Claim 33, lines 5-8, the phrase "said contact between said first diffusion and said another diffusion extends over insulation between

said first transistor and said second transistor". Claim 38, line 2, the phrase "said gate structure is self-aligned to said channel".

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Alavi et al.

In regards to claim 1, Alavi et al. shows all the elements of the claimed invention in figs. 1-43. It is a vertical field effect transistor, including: a semiconductor pillar conduction channel (n-Si), gate electrodes (POLY) [30] in trenches adjacent the semiconductor pillar [22, 24, 20], a layer of insulator (ILD) [44] adjacent the gate electrodes and opposite said semiconductor pillar, sidewalls (OXIDE) adjacent said semiconductor pillar above said gate electrodes in said trenches, insulator material [44] in said trenches above said gate electrodes and adjacent said sidewalls, said insulator material [44] being selectively etchable relative to said sidewalls and said semiconductor pillar.

In regards to claim 2, Alavi et al. further discloses isolation material [44] (outermost portion of layer [44]) adjacent said layer of insulator and surrounding said vertical

transistor, said isolation material being selectively etchable relative to said layer of insulator.

In regards to claim 3, Alavi et al. further discloses a contact [S] formed in an opening in said isolation material adjacent said layer of insulator to a conductive region [12] at an end of said pillar.

In regards to claim 4, Alavi et al. further discloses a contact [D] formed in an opening to an end of said pillar, and a contact [G1] formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall (sidewall spacer) [41] on said pillar.

In regards to claim 5, Alavi et al. further discloses a spacer [14] in said trench between said gate structure and a bottom of said trench.

In regards to claim 6, Alavi et al. shows all the elements of the claimed invention in figs. 1-43. It is an integrated circuit device, including: isolation material [44] surrounding transistor locations in a substrate [12], vertical field effect transistors [60] formed at said transistor locations and having a gate electrode structure (POLY) [30] formed in a trench, a layer of insulator material (ILD) in said trench between said isolation material [44] (outermost portion of layer [44]) and said gate electrode structure, said isolation material being selectively etchable relative to said layer of insulator material, and a contact opening [S] formed along an interface of said layer of insulator material and said isolation material.

In regards to claim 7, Alavi et al. shows said gate electrode structure includes dual gate electrodes extending on opposite sides of a conduction channel (n-Si).

In regards to claim 8, Alavi et al. shows a contact [S] formed in said contact opening in said isolation material adjacent said insulator material and extending to a conductive region [12] extending below said pillar.

In regards to claim 9, Alavi et al. shows a contact [D] formed in an opening to an end of said pillar, and a contact [G1] formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall [41] on said pillar.

In regards to claim 10, Alavi et al. shows a spacer [14] in said trench between said gate structure and a bottom of said trench.

6. Applicant's arguments filed 4/29/03 have been fully considered but they are not persuasive:

It is urged, in page 5 of the remarks, that page 16, line 6 of the specification discloses the gate extending on two or more sides of the conduction channel. However, page 16, line 6 only discloses the gate contacts can be formed on two or more different sides of the channel.

It is urged, in page 5 of the remarks, that page 21, line 21+ of the specification discloses a contact between two diffusions extending over the insulator. However, page 21, line 21+ never discloses the contact between said first diffusion and said another diffusion extends over insulation between said first transistor and said second transistor.

It is urged, in page 6 of the remarks, that page 12, line 7 of the specification discloses a gate structure self-aligned with the channel. However, page 12, line 7 only discloses the gate dielectric is formed self-aligned with the channel.

It is urged, in pages 6 and 7 of the remarks, that "sub-lithographic" is a well known terms. However, it is unclear as to what is the actual width of the channel as compare to the other structures of the device as claimed in claim 40.

It is urged, in pages 6 and 7 of the remarks, that sidewall spacers are another well-known structure which is commonly referred to as sub-lithographic. However, it is still unclear how the contact to said second diffusion comprises a spacer self-aligned to said edge as claimed in claim 30.

It is urged, in page 8 of the remarks, that Alavi teaches the contact openings of a vertical MOS structure are formed by lithographic etching of an interlayer dielectric layer and not "borderless" by being along existing insulators through selective etching of two insulating materials at their interface. However, the device of figures 24 and 39 can still read on claims 1-10. Claims 1-10 never discloses the contact openings of the MOS structure are borderless by being along existing insulators through selective etching of two insulating materials at their interface. Therefore, Alavi still reads on claims 1-10.

7. Claims 18-28, 31-39 and 41-44 are allowed.
8. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is a contact to the first diffusion borderless to the gate structure.
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl  
July 26, 2003

Steven Loke  
Primary Examiner

